IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Daniel E. Lenoski, et al.

Serial No.: 09/910,591

Filing Date: July 20, 2001

Group Art Unit: 2188

Examiner: Reginald G. Bragdon

Title: METHOD AND SYSTEM FOR MANAGING MEMORY

IN A MULTIPROCESSOR SYSTEM

Commissioner of Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Applicant respectfully requests, pursuant to 37 C.F.R. \$\$1.56, 1.97, and 1.98, that the documents listed on the attached Form PTO-1449 be considered and cited in the examination of the above-identified application. A copy of these documents are enclosed for the convenience of the Examiner. Furthermore, pursuant to 37 C.F.R. \$\$1.97(g) and (h), Applicant makes no representation that these documents qualify as prior art or that these documents are material to patentability of the present application or that a search has been made.

REMARKS

An Office Action has been received by the Applicant in the above identified patent application. Pursuant to 37 C.F.R. §1.97(c) enclosed herewith is a check for \$180.00. Please charge any fees or credit any overpayment to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,

BAKER BOTTS L.L.P.

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Dear Sir:

CERTIFICATE OF MAILING BY EXPRESS MAIL

I hereby certify that the attached Request for Continued Examination with check and Information Disclosure Statement with Form PTO-1449 are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on this 11th day of February 2005, addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Willie Jiles

Express Mail Receipt No. EV 323311622 US

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| PTO-1449 | Application No. 09/910,591 | | Applicant(s) Daniel E. Lenoski, et al. | | |
| Information Disclosure Citation In an Application | Docket Number 062986.0211 | Group Art Unit 2188 | | Filing Date 07/20/01 | |

| CER 1 | U.S. PATENT DOCUMENTS U.S. PATENT DOCUMENTS CLASS SUBCLASS FILING DATE 6,085,263 07/04/00 Sharma, et al. | | | | | | | |
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| | DOCCMENT | | | VII. | | YES | NO |
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| 0 | | | | | | | |

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| | Culler, et al. "Parallel Computer Architecture", San Francisco Morgan-Kaufman, cover pages and pp. 553-559. | 1998 |

DATE CONSIDERED

EXAMINER

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

U.S. PATENT AND TRADEMARK OFFICE